IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Behrens et al.
Serial No.:	10/032,513
For:	DATA FLOW SYNCHRONIZATION
Filed:	26 OCT 2001
Examiner:	Juan A. Torres
Art Unit:	2631
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Attorney Docket No.: 20 01 0631

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants are submitting the present document concurrently with a notice of appeal for the above-noted application. Applicants are requesting that the Office review the final rejection of the as set forth in a final office action dated 2 AUG 2005. No amendments are being filed with this request.

Status of the Claims

Claims 1 – 9 are pending in the application, and stand finally rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,893,072 to Matsumoto (hereinafter "the

Matsumoto patent") in view of U.S. Patent No. 6,055,285 to Alston (hereinafter "the Alston patent").

Clear Errors in the Examiner's Rejection

The final office action indicates that the Matsumoto patent discloses a receiving unit and a signal generator, and that the Alston patent discloses a synchronizing unit. The final office action then asserts that the Matsumoto and Alston patents, in combination, disclose the elements of claim 1.

In a response mailed 2 NOV 2005, from the top of page 3, to the middle of page 4, Applicants explained that:

(1) there is no motive to modify the system of the Masumoto patent to include the synchronizer of the Alston patent; and

(2) a modification of the Matsumoto patent to provide clocks from more than a single generator would change the principle of operation of the system in the Matsumoto patent.

The Matsumoto patent is directed toward a problem encountered when a signal is transmitted through a multistage logic circuit under control of a clock signal. In such a circuit, a time delay shift of the signal occurs, where the time delay is associated with the period of the clock signal (col. 1, lines 44 – 48). Consequently, the delay time of a signal to-be-measured is different from the delay time of an expected signal (col. 1, lines 48 – 53). The Masumoto patent discloses a solution for this problem by employing an apparatus in which the expected signal passes through transferring circuits, the number of which is equal to the number of clocked logic circuits (col. 3, lines 24 – 41).

FIG. 2 of the Matsumoto patent shows an embodiment of an apparatus that includes a logic circuit section having a plurality of flip-flops 30, 31, 32 and 33 operating under the control of a timing signal from a timing generator (TG) (col. 4, lines 34 – 36). The apparatus transmits an expected signal through a plurality of flip-flop circuits F11 – Fnn (col. 4, lines 53 – col. 4, line 4) such that the expected signal can be delayed a desired number of times (col. 5, lines 6 – 8). Thus,

data transmitted through the plurality of flip-flops 30, 31, 32 and 33 is synchronized with the expected signal transmitted through the plurality of flip-flop circuits F11 – Fnn (see col. 3, lines 35 – 38).

FIG. 5 of the Matsumoto patent shows an embodiment in which the timing generator TG generates two clocks, namely ck1 and ck2, that have the same repetition period but are different in phase from each other (col. 7, lines 52 – 54). The Matsumoto patent states that the embodiment of FIG. 5 operates similarly to the embodiment of FIG. 2 (col. 7, lines 61 – 65). Thus, in the embodiment of FIG. 5, data transmitted through a plurality of flip-flops 301 - 332 is synchronized with an expected signal transmitted through the plurality of flip-flop circuits F11 – Fnn.

The Alston patent is directed toward a synchronization circuit for synchronizing a transfer of data between two asynchronous circuits (col. 1, lines 7 - 10).

The final office action, on page 6, states that the suggestion/motive for supplementing the apparatus of the Matsumoto patent with the synchronization circuit of the Alston patent is "to synchronize two clock domains of the signal generator and the response from the DUT." Applicants respectfully submit that this cited combination of the Matsumoto and Alston patents is improper for purposes of a section 103(a) rejection of the claims.

The Matsumoto patent explains that the embodiments of both of FIG. 2 and FIG. 5, synchronize data. As such, the apparatuses of the Matsumoto patent do not have the problem that the Alston patent is intended to solve. That is, whereas the apparatuses of the Matsumoto patent synchronize the data, there is **no motive** for modifying the apparatus of the Mastsumoto patent with the synchronizer of the Alston patent.

Furthermore, in the Matsumoto patent, in each of FIGS. 2 and 5, all clocks are provided by the timing generator TG. In FIG. 2, there is only one clock, and as such, there is no need to synchronize two clock domains. In FIG. 5, the two clocks (ck1 and ck2) have a fixed, out-of phase relationship that is specifically set by the timing generator (TG), to co-operate with one

another, for the purpose of synchronizing data. Applicants respectfully submit that altering the clock configurations of either of FIGS. 2 or 5, to include the synchronizer of the Alston patent, "to synchronize two clock domains", as suggested by the final office action, would **change the principle of operation** of the Matsumoto patent.

For the reasoning provided above, Applicants respectfully submit that the cited combination of the Matsumoto and Alston patents is improper for purposes of a section 103(a) rejection of the claims of the present application.

Respectfully submitted,

12/7/05
Date

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